



DOEACC CENTRE CALICUT
COURSE PROSPECTUS

Name of the Group: *VLSI*

Name of the Course: *PG Diploma in VLSI & Embedded Hardware Design*

Course Code: *VL 500*

Starting Date: *30th August 2010*

Duration: *24 weeks*

Preamble: VLSI (Very Large Scale Integration) technology has emerged as a very important technology to provide tremendous quantum of processing power and functionality to modern electronic systems. Ubiquitous Computing and Embedded Systems, based on VLSI are revolutionizing every walks of our daily lives, be it Consumer Electronics, Communication, Computing, Automation, Space Application, Defense and to just about everything. With the advancements in silicon processing technologies for MEMS, NEMS and RF components, many of the formerly external components can now be integrated into a single System-on-Chip which has resulted in a dramatic improvement in performance while achieving reduction in the size, cost and power consumption. Complexity in such systems arises not only from the diversity of the technologies, from sensors and actuators to base-band DSP software, etc., that must be integrated on-chip, but also from the fact that such systems must be increasingly built from parts that have been designed separately and using different tools and flows.

Objectives of the Course: The PG Diploma in VLSI & Embedded Hardware Design is intended to impart training in designing complex embedded systems using reusable Intellectual Property (IP) Cores as building blocks and employing hierarchical design methods. Emphasis of the teaching curriculum is on design methodology and practical applications. The course contents have been designed keeping in view the requirements for skilled manpower.

The curriculum has been designed in consultation with industry and academic experts and our strategic partners, to map the skill sets and design methodologies, which is high in demand in VLSI & Embedded Systems industries. Our students have been successfully placed in reputed companies and we enjoy the trust of many reputed companies, who have entered into strategic alliances with us.

Outcome of the Course: This course is frequently updated in synchronization with the industry to provide the trainees in-depth knowledge and skills required by Embedded & VLSI markets around the globe. It provides comprehensive understanding about the fundamental principles, methodologies and industry practices.

This uniquely hybrid course makes the successful participants readily employable in multiple roles available in broad spectrum of relevant industries. For people interested in entrepreneurship this would be an excellent launch pad. In addition the course serves as a concrete platform for people involved in application research, consultancy and high end product development in both industry and academia.

Course Structure:

The VL500 contains ten modules. The students are required to do a project work for a period of 7 weeks to be eligible for issue of PG Diploma in VLSI and Embedded Hardware Design.

VL 500	Module Name	Duration
VL 501	Advanced Digital Design	3 weeks
VL 502	VHDL - Language and Coding for Synthesis	3 weeks
VL 503	Verilog - Language and Coding for Synthesis	3 weeks
VL 504	CMOS Logic Design	1 week
VL 505	Embedded Controller Based System Design	1 weeks
VL 506	Programmable SoC	1 week
VL 507	Embedded Product Design	1 week
VL 508	FPGA Design Methodology and Prototyping	2 week
VL 509	RTL Verification	1 week
VL 510	Project	7 weeks

Other Contents

- a. **Course Fees:** Course Fee is Rs. 48000/- (All inclusive). The course fee can be paid in three installments.

Course Fees:

Total course Fee is Rs. 48000/- (All inclusive). SC/ST candidates and Physically Handicapped candidates are eligible for fee concession as per rules.

The course fee can be paid in three installments.

First Installment: Rs. 10000/-

The students in the **first selection list** have to pay the first installment fee at the time of taking provisional admission itself (after selection).

The students in **the additional selection list** have to pay both the first & second installment fee together on the date of counseling.

Second Installment: Rs. 20000/-

Second installment has to be paid on the date of counseling.

Third Installment: Rs. 18000/-

Third installment has to be paid on or before 15th Nov 2010.

- b. **Eligibility:** BE /B.Tech in Electronics/ Electronics & Communication/ Electrical/ Instrumentation/Computer Science or M.Sc (Electronics). Diploma students* may also be considered. Graduates with appropriate experience and final year students[#] also may apply

[#] Final year students have to include the copies of course completion certificate of their qualifying degree/ diploma or copies of the mark lists up to the last semester/ year. On the date of counseling/ admission, he/she must produce the originals of course completion certificate/ mark lists up to the last semester/year examination.

*Diploma Students will be eligible only for Advance Diploma in VLSI and Embedded Hardware Design.

- c. **Number of Seats:** 40

SC/ST candidates and Physically Handicapped candidates are eligible for seat reservation and relaxation in the minimum marks for eligibility.

d. How to Apply :

Procedure for Online application: Students can apply online by filling up the online application form. The students are first required to obtain the DD for Rs.1000/- towards advance fee and Rs.500/- in case hostel is required. The students are required to fill the details with regards to the DD Number, Date and amount. The students are requested to note down their registration number allotted after pressing the "Submit" button and forward the demand draft mentioning their name and their online registration number. Online registrations not containing the advance fee details will not be considered for registration.

Procedure for applying using the Application form: The students can download the application form from our web site and fill the particulars and forward the same to the Training Officer along with the requisite fee as mentioned above.

Filled in application forms and Demand Draft should be sent to the **Training Officer, DOEACC Centre Calicut, P. B. No. 5, NIT Campus Post, CALICUT – 673 601, Kerala. The Name of the Course Applied for should be super scribed on the top of the cover in which the application form is forwarded.**

e. Selection of candidates:

Candidates will be selected based on their marks in their qualifying examination subject to eligibility and availability of seats. Selection of candidates who have completed the course but expecting the results shall be based on the availability of seats. All selected candidates shall be intimated of their selection by **email alone**. The list of selected candidates shall be published in our website

List of selected students will be published in our website, students are advised to visit our website to satisfy themselves of their selection.

First selection list will be prepared based on the applications received on or before 9th August 2010. The **additional selection list** will be prepared, if there are vacant seats, based on the applications received on or before 25th August 2010 and excluding the applicants included in the first selection list.

First selection list: The first selection list of applicants will be finalized and published in our website on 10th August 2010. After that seats will be available only against any vacancy that arises and will be published in the **additional selection list**.

Mode of fee Payments : (Any 1 of the 3 options given below may be used to pay the fees)

1. Demand Draft to be drawn in favor of Director, DOEACC Center Calicut, Payable at State Bank of India, Calicut NIT Branch(2207).
2. Using the pay in slip available in our web site, through any branch of SBI (where this format is accepted). The **original counterfoil** should reach here before the last date to apply.
3. The fees can be paid by DD or can be paid directly into our account from any bank where core banking facility is available. The details required for direct payment are as given below.

Current Account No:	:	010401158037
Bank Name	:	SBI, NITC Chathamangalam
Bank Code	:	2207
IFSC No	:	SBIN0002207

The depositor should obtain the **UTR Number** from the branch while depositing cash directly into our account. Depositor should also obtain the acknowledgement duly filled up and signed by the staff of the bank through which the amount was deposited. UTR number should be mentioned in all the correspondences to us pertaining to amount. The following details are to be given by the depositor.

1. Name of the Depositor
2. Name of the Student
3. Date of Payment
4. Amount Deposited
5. Name of Bank/branch through which amount deposited
6. Purpose – Course ID – Advance Fee/Hostel Rent/Installment Fee etc.
7. Proof of Deposit (counterfoil/acknowledgement in **original**)
8. UTR Number

The Centre will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account

f. Test/Interview (if applicable) : N/A

g. Counseling/Admission: 30-August-2010.

h. Admission Procedure :

Students who have been selected for test/interview/counseling/admission are required to report to the Centre on the prescribed day by 9:30 hrs along with the following

1. Attested Copies of Proof of Age, Qualifications, etc
2. Original Certificate of the above

3. Two copies of photograph and one stamp size photograph for identity card.
4. SC/ST Certificate in English/Hindi (if applicable)
5. Income Certificate in English/Hindi (if applicable)

The students on reaching the Centre are required to meet the Front Office Councilor (FOC). The FOC then directs the student to the Course Coordinator. The student gets the enrollment form verified by the Course Coordinator and then meets the FOC who shall direct the student to the Accounts section for payment of fees. A student is thus admitted.

- i. **Discontinuing the course:** No fees under any circumstances shall be refunded in the event of a student discontinuing the course. A student can however, be eligible for module certificates (applicable only for courses which provide for modular admission) for modules he has successfully completed provided he has paid the entire course fees.
- j. **Course Timings:** The classes and labs are from 9.30 am to 12.30 pm and 1.30 pm to 5.15 pm Monday to Friday.

k. Location and How to reach :

DOEACC CENTRE Calicut is located very near to NIT (REC) campus and is about 22Kms from the Calicut (Kozhikode) city. A number of buses [Buses to NIT via Kunnamangalam] are available from "Palayam Bus Stand or KSRTC Bus Stand". Our stop is called "Pandrandu" & is one stop before NIT. The bus fare is Rs.11/- from Calicut City to DOEACC Centre and is on the right side.

Calicut (Kozhikode) is well connected by Rail, Road and Air from different parts of the country. The climatic conditions in Calicut are perhaps one of the best in India throughout the year. The maximum and minimum temperatures range between 35 and 20°C. The cool breeze further adds to the comfort.

l. Course enquiries :

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm).

m. IMPORTANT DATES :

Last date for receiving completed application forms	First selection list will be prepared based on the applications received on or before 9th August 2010.
	The additional selection list will be prepared based on the applications received on or before 25th August 2010 and excluding the applicants included in the first selection list.
Publication of first selection list in our Website http://www.doeaccalicut.ac.in	10/08/2010

Last date for taking provisional admission by paying the first installment of fees for applicants in the first selection list	17/08/2010
Publication of additional selection list in our website (if there are vacant seats)	25/08/2010
Counseling date	30/08/2010
Class Commencement date	31/08/2010
Payment of first installment of fees for applicants in first selection list	On or before 17/08/2010
Payment of second installment fees for applicants in first selection list	On 30/08/2010
Payment of first & second installment fees for applicants in additional selection list	On 30/08/2010
Payment of third installment fees	On or before 15/11/2010

n. Placement: We have a placement cell, which provides placement assistance to students who qualify our courses. Partial List of placement is given in our webpage <http://www.doeaccalicut.ac.in/html/vlsi.html>

o. Hostel facilities :

Hostel accommodation is available for boys and girls on daily or monthly chargeable basis. The hostel fee varies from Rs.450/- to Rs.900/- per month depending on the location of accommodation. However, students are required to pay the hostel fees for the duration of the course for which they are seeking admission at the time of joining the course.

p. Canteen facilities :

The Centre has a canteen functioning at the main campus and food at reasonable rates is available for breakfast, lunch, and dinner

q. Lab Facilities :

DOEACC – CYPRESS Semiconductor JOINT PSoC Lab.

FPGA Development Kits from Xilinx.

FPGA Development Kits from Altera.

Xilinx ISE, Quartus II

Programmable SoC Solutions from Cypress Semiconductors

Complete range of Simulation, Synthesis Tools from Mentor Graphics

FPGA Design and Verification Tools

ASIC Design and Verification Tools

Hardware-Software Co-verification Tools

IC Nanometer Design Tools (Back end tools)

System Modeling Tools

Mentor Graphics PADS Logic, KeilC from ARM.

Microcontroller Development Kits. Logic Analyser, SMD Rework-station

Digital Storage & Mixed Signal Oscilloscopes

r. Course Contents :**1. Advanced Digital Design**

- a. Combinational Circuit Design
- b. Sequential Circuit Design
- c. Design of controller and Datapath units
- d. State Machines
- e. Controller Design using FSMs & ASMs
- f. Design Examples & Case Studies

2. VHDL - Language and Coding for Synthesis

- a. Language Constructs, Data types
- b. Design Styles
- c. Behavioral Modeling, Dataflow Modeling
- d. Structural Modeling
- e. Generics and Configurations
- f. Subprograms and overloading
- g. Packages and Libraries
- h. Advanced features of VHDL
- i. Test Bench Design and Coding
- j. Synthesis issues
- k. Mini Project and Case Studies

3. Verilog - Language and Coding for Synthesis

- a. Introduction to Verilog HDL & Hierarchical Modeling Concepts
- b. Lexical Conventions & Data Types
- c. System Tasks & Compiler Directives
- d. Modules, Ports and Module Instantiation Methods
- e. Gate Level Modeling
- f. Dataflow Modeling
- g. Behavioral Modeling
- h. RTL Design and Logic Synthesis and Synthesis issues
- i. Design Verification using Test benches
- j. Mini-project and Case Studies

4. CMOS Logic Design

- a. MOS Fundamentals
- b. MOS Switches & Designs
- c. Transmission Gates
- d. Inverter - DC, AC Characteristics
- e. Combinational and Sequential Logic
- f. Introduction to Layout Tools

5. Embedded Controller Based System Design

- a. Basic Electronics
- b. Intel 8x51 Architecture
- c. Embedded C
- d. Peripheral Interfacing – LCD, Keyboard, LEDs/ Buzzer/ Relays
- e. 7 Segment LED, ADC, DAC, Serial Port, EEPROM, RTC.
- f. Lab sessions based on Keil C
- g. Use of test and measuring instruments

6. Programmable SoC

- a. Introduction to Programmable SoC
- b. PSoC Designers IDE
- c. Design examples using PSoCs

7. Embedded Product Design

- a. Quality Principles & Tools
- b. Product Development Process
- c. Interconnection Design & EDA Tools Mentor graphics/ORCAD
- d. Designing for Electromagnetic Compatibility
- e. Thermal Design
- f. Documentation
- g. Industrial Design
- h. Project Management
- i. Team Work and Communication

8. FPGA Design Methodology and Prototyping

- a. Introduction to Programmable Logic and FPGAs
- b. Popular CPLD & FPGA Families
- c. Architecture of popular Xilinx and Altera FPGAs
- d. FPGA Design Flow Altera Quartus II
- e. FPGA Design Flow Xilinx ISE
- f. Implementation Details.
- g. Advanced FPGA Design tips
- h. Logic Synthesis for FPGA
- i. Placement & Routing
- j. Static Timing Analysis
- k. Design problems using Xilinx Platforms
- l. Design problems using Altera Platforms
- m. Case Studies on FPGA Based implementations
- n. IP Reuse Methodology
- o. Soft IP vs Hard IP
- p. IP Design Process
- q. System Integration with reusable IP

9. RTL Verification

- a. Functional Verification – Concepts
- b. Simulators, Coverages and Metrics
- c. Various Verification Methodologies - OVM & VMM
- d. Testing strategy - Directed and random Testing
- e. Test Cases Vs Test Benches
- f. High Level Modeling & OOPs – Concepts
- g. Stimulus Generation Bus Function Models & Response Monitors-
Overview
- h. Introduction to HVLs-SystemC
- i. Case study of an IP (block level Verification Only)

10. Project